Category	Instruction	Oprands	Operation	Opcode	Fields
No-operation	nop	N/A	none	00 00 00	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ
	add	rt,ra,rb	rt <= ra + rb	00 10 00	ΦΦ ΦΦΦΦ ΦΦΦΦ BBBB BAAA AAΦT TTTT
	sub	rt,ra,rb	rt <= ra – rb	00 01 00	ΦΦ ΦΦΦΦ ΦΦΦΦ BBBB BAAA AAΦT TTTT
	addi	rt,ra,imm	rt <= ra + immediate value	00 10 01	II IIII IIII IIII ΦAAA AAΦT TTTT
	subi	rt,ra,imm	rt <= ra – immediate value	00 01 01	II IIII IIII IIII ΦAAA AAΦT TTTT
	inc	rt,ra	rt <= ra + 1	00 10 10	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
Arithmetic	dec	rt,ra	rt <= ra – 1	00 01 10	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	not	rt,ra	rt <= NOT ra	01 11 11	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	and	rt,ra,rb	rt <= ra AND rb	01 01 00	ΦΦ ΦΦΦΦ ΦΦΦΦ BBBB BAAA AAΦT TTTT
	or	rt,ra,rb	rt <= ra OR rb	01 10 00	ΦΦ ΦΦΦΦ ΦΦΦΦ BBBB BAAA AAΦT TTTT
	xor	rt,ra,rb	rt <= ra XOR rb	01 11 00	ΦΦ ΦΦΦΦ ΦΦΦΦ BBBB BAAA AAΦT TTTT
	andi	rt,ra,imm	m rt <= ra AND immediate value	01 01 01	II IIII IIII IIII ΦAAA AAΦT TTTT
	ori	rt,ra,imm	rt <= ra OR immediate value	01 10 01	II IIII IIII IIII ΦAAA AAΦT TTTT
	xori	rt,ra,imm	rt <= ra XOR immediate value	01 11 01	II IIII IIII IIII ΦAAA AAΦT TTTT
	shl	rt,ra,n	rt <= ra shifted left by n bits	01 00 01	ΦΦ NNNN ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	shr	rt,ra,n	rt <= ra shifted right by n bits	01 00 00	ΦΦ NNNN ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	rol	rt,ra,n	n rt <= ra rotated left by n bits	01 00 11	ΦΦ NNNN ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
Logic	ror	rt,ra,n	rt <= ra rotated right by n bits	01 00 10	ΦΦ NNNN ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	move	rt,ra	rt <= ra	10 00 00	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	loadi	rt,addr	rt <= DMEM[addr] {direct addressing}	10 01 01	AA AAAA AAAA AAAA AAAA AAΦT TTTT
	loadr	rt,ra	rt <= DMEM[ra] {register indirect addressing}	10 01 10	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
	loado	rt,ra,off	rt <= DMEM[ra+off] {base plus offset addressing}	10 01 11	OO OOOO OOOO OOOO ΦAAA AAΦT TTTT
	stori	rt,addr	DMEM[addr] <= rb {direct addressing}	10 10 01	AA AAAA AAAA AAAA AAAA AAΦT TTTT
	storr	rt,ra	DMEM[ra] <= rb {register indirect addressing}	10 10 10	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
Transfer	storo	rt,ra,off	DMEM[ra+off] <= rb {base plus offset addressing}	10 10 11	OO OOOO OOOO OOOO ΦAAA AAΦT TTTT
	jmp	off	Jump to IMEM[PC+off]	11 00 00	OO OOOO OOOO OOOO OOOO OOOO OOOO
control	brc	ra,cond,off	f If condition is true, then jump to IMEM[PC+off], else continue Conditions: ra = 0 ; ra ≠ 0 ; ra = 1; ra < 0; ra > 0; ra ≤ 0; ra ≥ 0	11 10 00	OO OOOO OOOO OOOO ΦAAA AAΦΦ ΦCCC

Operands	Fields
rt,ra,rb	ΦΦ ΦΦΦΦ ΦΦΦΦ BBBB BAAA AAΦT TTTT
rt,ra,off	OO OOOO OOOO OOOO ΦAAA AAΦT TTTT
rt,ra,n	ΦΦ NNNN ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
rt,ra,imm	II IIII IIII IIII ΦAAA AAΦT TTTT
rt,ra	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦAAA AAΦT TTTT
rt,imm	II IIII IIII IIII IIII IIΦT TTTT
ra,cond,off	OO OOOO OOOO OOOO ΦAAA AAΦΦ ΦCCC
rt,addr	AA AAAA AAAA AAAA AAAA AAΦT TTTT
off	OO OOOO OOOO OOOO OOOO OOOO OOOO
N/A	ΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ

Spec	num	bits
Instruction	4.29E+09	32
opcode	64	6
data size	65536	16
registers	32	5
data offset	512	9
instruction	256	8
max shift	16	4
flags	7	3