UNIVERSITY of York

DEPARTMENT OF ELECTRONICS

COMPUTER ARCHITECTURES

Homework Two

Abstract

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1   Question 1

A Flowchart of the algorithm for paged segmentation, assuming the presence of separate translation look aside buffers (TLBs) for pages and segments.
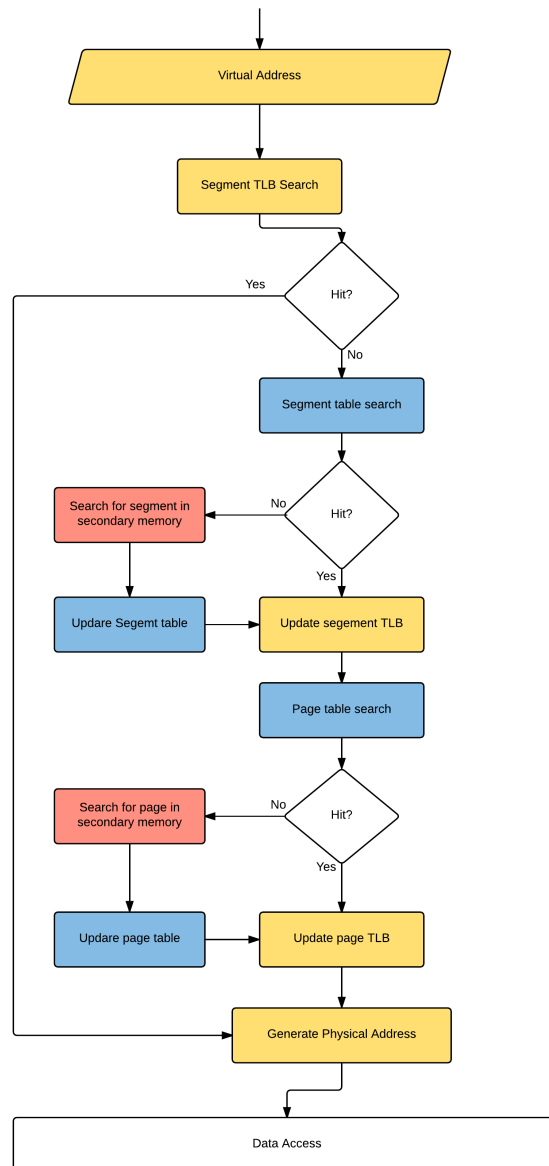

Figure 1: Flowchart for paged seqmentation

2   Question 2

$addresssize = 32b$

$blockssize = 64words = 2048b$

$wordsize = 32b$

$cachesize = 16kB = 131072b$

$numblocks = cachesize/blocksize = 64$

2.1   direct-mapped cache

2.1.1   sizes

Offset : $size(\text{offset}) = (blocksizeB/wordsizeB) + wordsizeB = (256/32) + 4 = 12b$

Index : $size(\text{index}) = log_2(cachesize/blocksize) - 1 = log_2(16kB/256B) - 1 = 8b$

Tag : $size(\text{tag}) = addresssize - size(\text{offset}) - size(\text{index}) = 32 - 12 - 8 = 12b$

2.1.2   hits and misses

2.2   fully-associative cache

2.2.1   sizes

Offset :   The same as direct mapped cache $= 12b$

Index :   Fully associative cache dose not have an index $0b$

Tag : $size(\text{tag}) = addresssize - size(\text{offset}) = 32 - 12 = 20b$

2.2.2   hits and misses

2.3   set-associative cache with 2 blocks per set

2.3.1   sizes

Offset :   The same as direct mapped cache $= 12b$

Index : $size(\text{index}) = log_2(\text{numsets}) - 1 = log_2(\text{blocksize}/2) - 1 = 4$

Tag : $size(\text{tag}) = addresssize - size(\text{offset}) - size(\text{index}) = 32 - 12 - 4 = 16b$

2.3.2   hits and misses

2.4   set-associative cache with 8 blocks per set

2.4.1   sizes

Offset :   The same as direct mapped cache $= 12b$

Index : $size(\text{index}) = log_2(\text{numsets}) - 1 = log_2(\text{blocksize}/8) - 1 = 2$

Tag : $size(\text{tag}) = addresssize - size(\text{offset}) - size(\text{index}) = 32 - 12 - 2 = 18b$

2.4.2   hits and misses

3   Question 3

Appendices