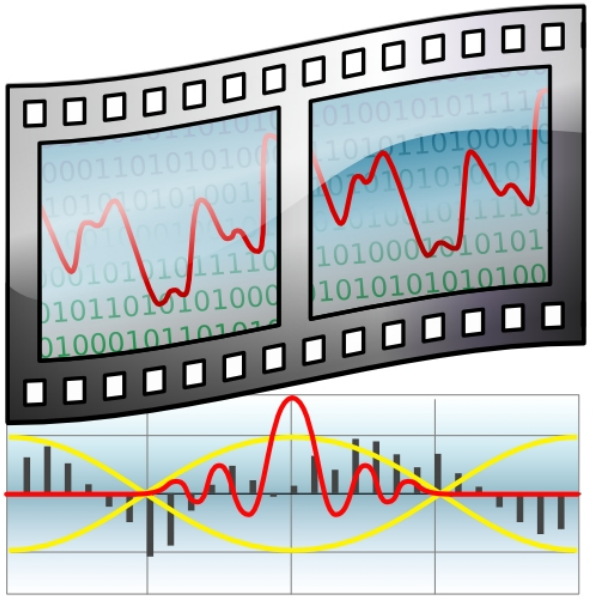
Theora Hardware Decoder



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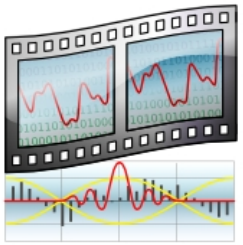
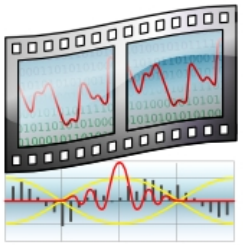


Profile Analisys

Simple Profile Analisys made with *gprof* :

% time	cumulative seconds	self seconds	calls	self ms/call	total ms/call	name
14.88	21.08	21.08	3597	5.86	39.33	LoadAndDecode
10.52	35.99	14.91	9847971	0.00	0.00	**FilterHoriz**
10.51	50.88	14.89	3537252	0.00	0.00	**ReconInterHalfPixel2**
9.61	64.50	13.62	9861274	0.00	0.00	**FilterVert**
9.12	77.42	12.92	3597	3.59	29.22	ReconRefFrames
8.74	89.80	12.38	2905949	0.00	0.00	**ReconInter**
7.67	100.67	10.87	2809557	0.00	0.00	**IDct10**
5.19	108.03	7.36	845503	0.01	0.01	**IDctSlow**
4.33	114.16	6.13	21614069	0.00	0.00	ExtractToken
3.33	118.88	4.72	2080037	0.00	0.00	**ReconIntra**
2.77	122.81	3.93	7889638	0.00	0.01	**ExpandBlock**
2.15	125.85	3.04	3597	0.85	1.38	QuadDecodeDisplayFragments
2.10	128.83	2.98	4868178	0.00	0.00	**IDct1**
1.88	131.49	2.66	5361174	0.00	0.00	CopyBlock
1.85	134.11	2.62	18575043	0.00	0.00	ExpandToken
1.40	136.09	1.98	3597	0.55	8.48	**LoopFilter**



Profile Analisys

Functions that are interesting to be implemented in hardware :

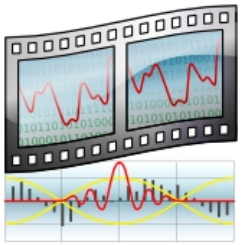
```
LoopFilter
FilterHoriz
FilterVert

ReconInterHalfPixel2
ReconInter
ReconIntra

IDct10
IDctSlow
IDct1

ExpandBlock
```

Total cpu-time percentage consumed by these functions: 61 %



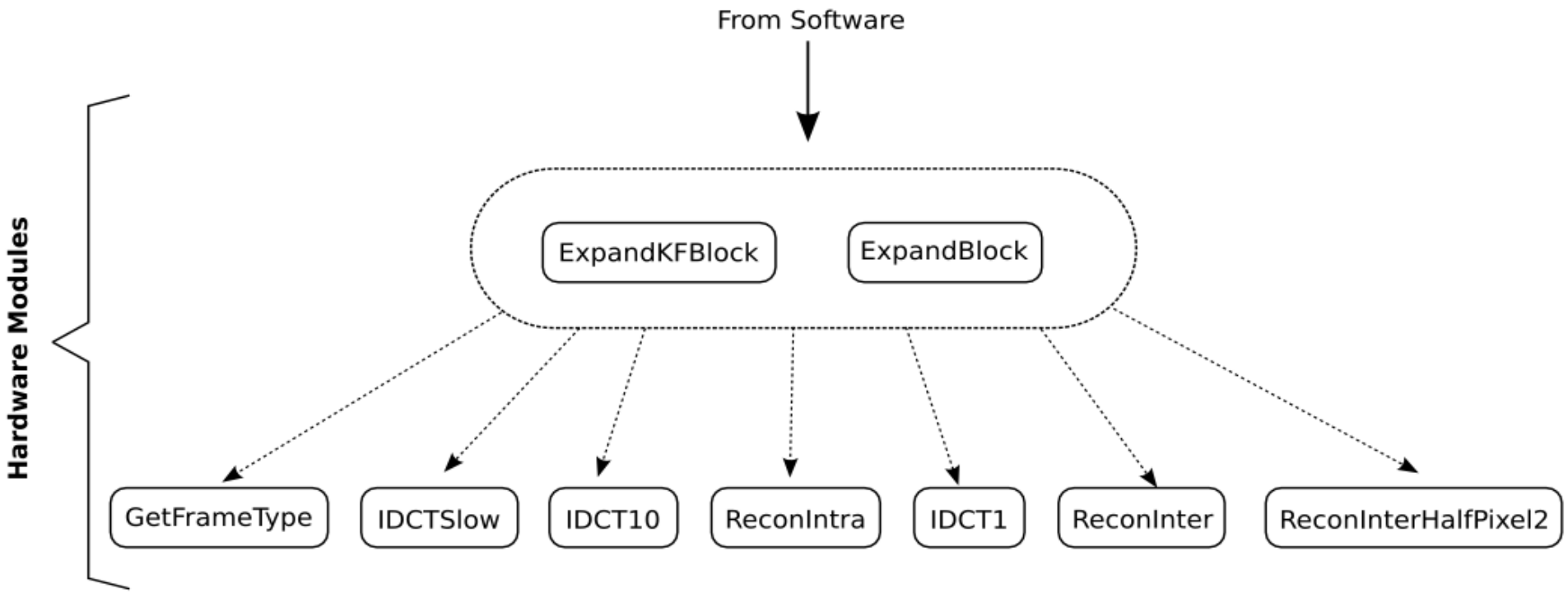
Profile Analisys

These functions are interesting to be implemented in hardware because they are :

- **very data-path intensive,**
- **very cpu-time consumer,**
- **and are self-contained, isolated from other functions**

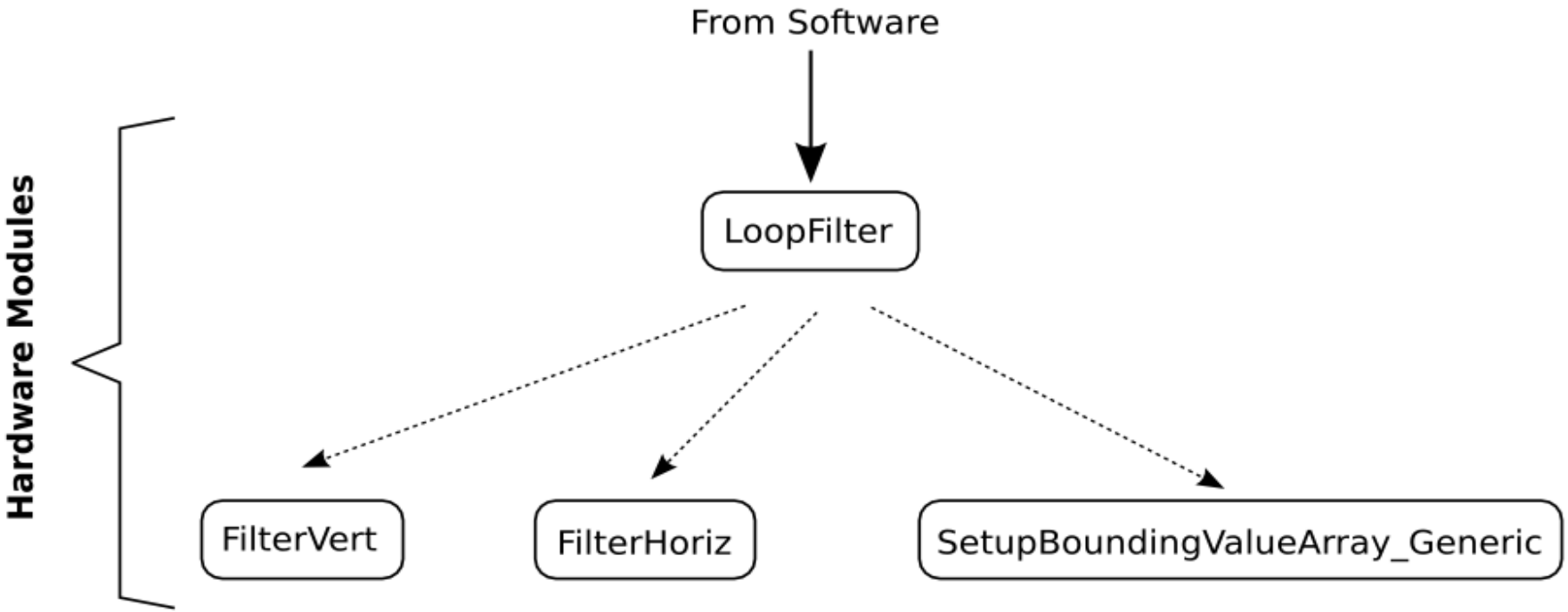
Data-path / pipeline

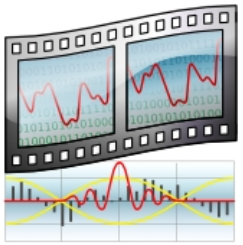
Piece of the call-graph:



Data-path / pipeline

Piece of the call-graph:





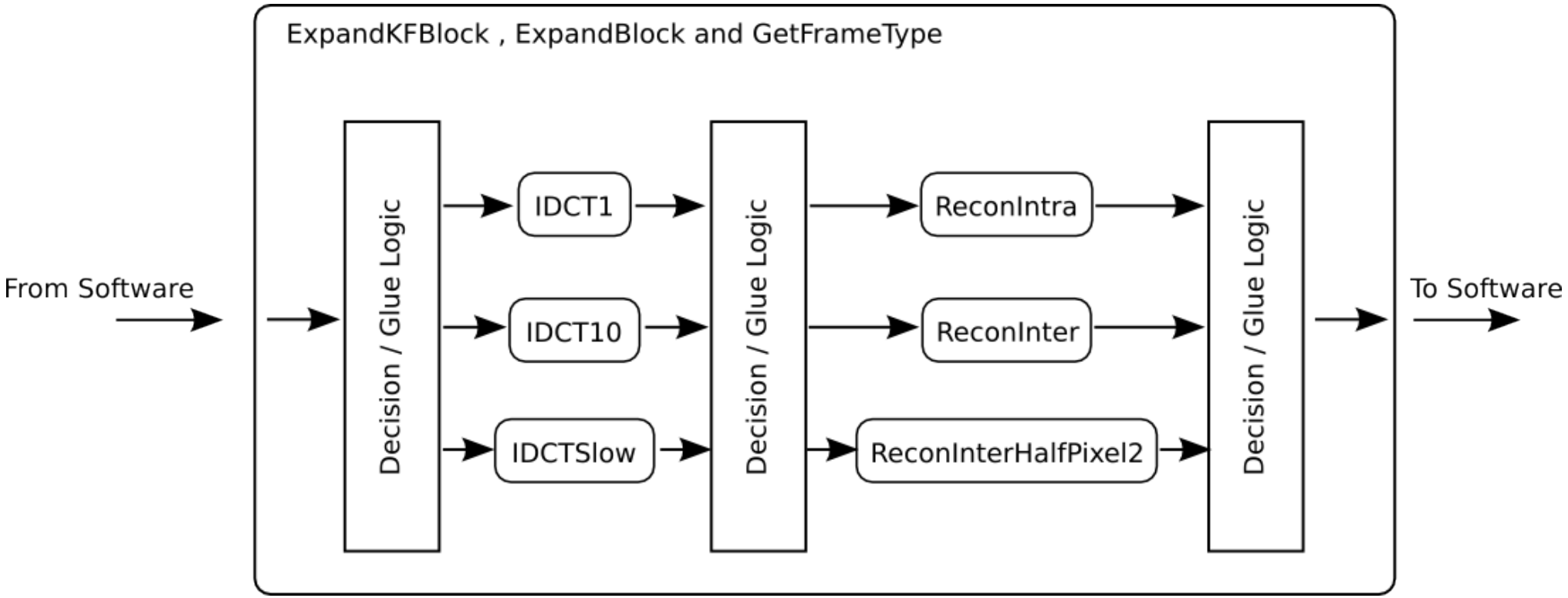
Data-path / pipeline

These two branches of the call-graph are independent and sugest us the implementation of two independent acceleration pipelines

Data-path / pipeline

Pipeline 1

Sub-Modules:

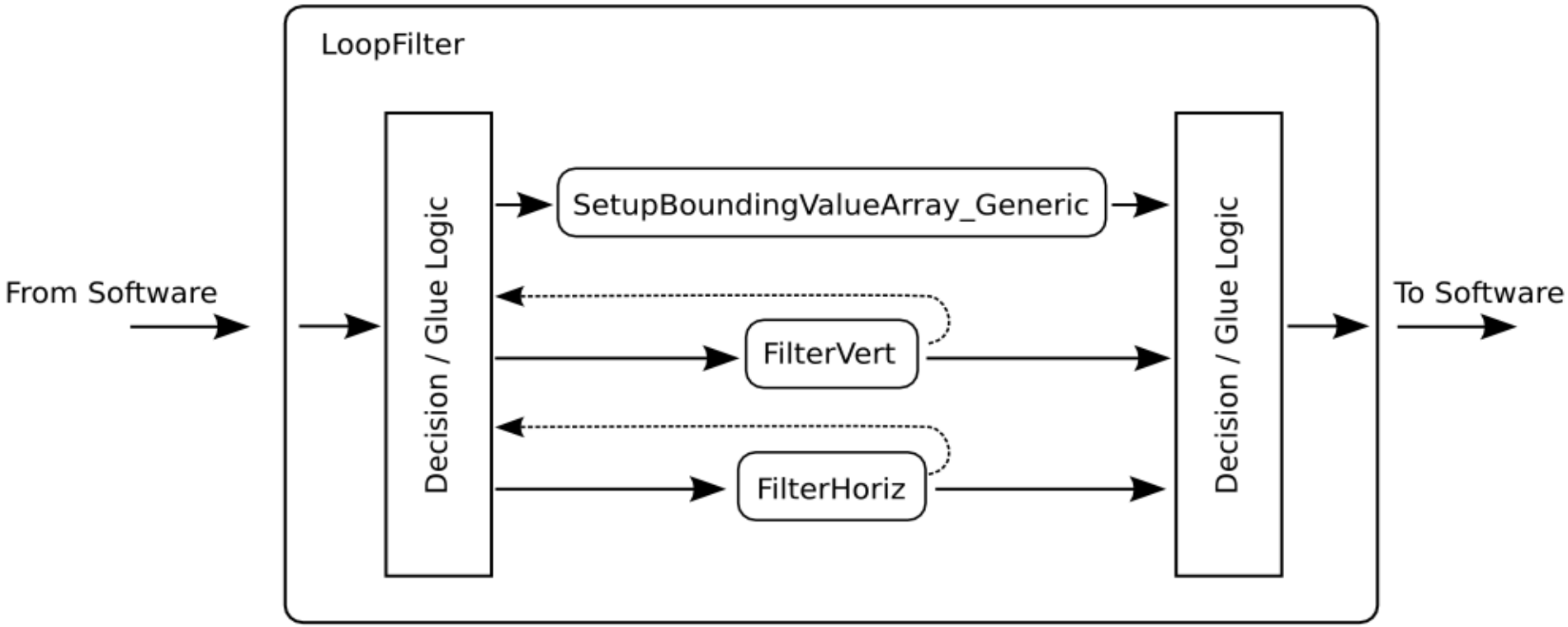


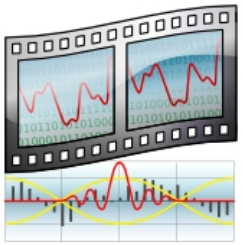
ExpandKFBlock and ExpandBlock will be merged into same pipeline and a Decision logic will control the pipeline

Data-path / pipeline

Pipeline 2

Sub-Modules:



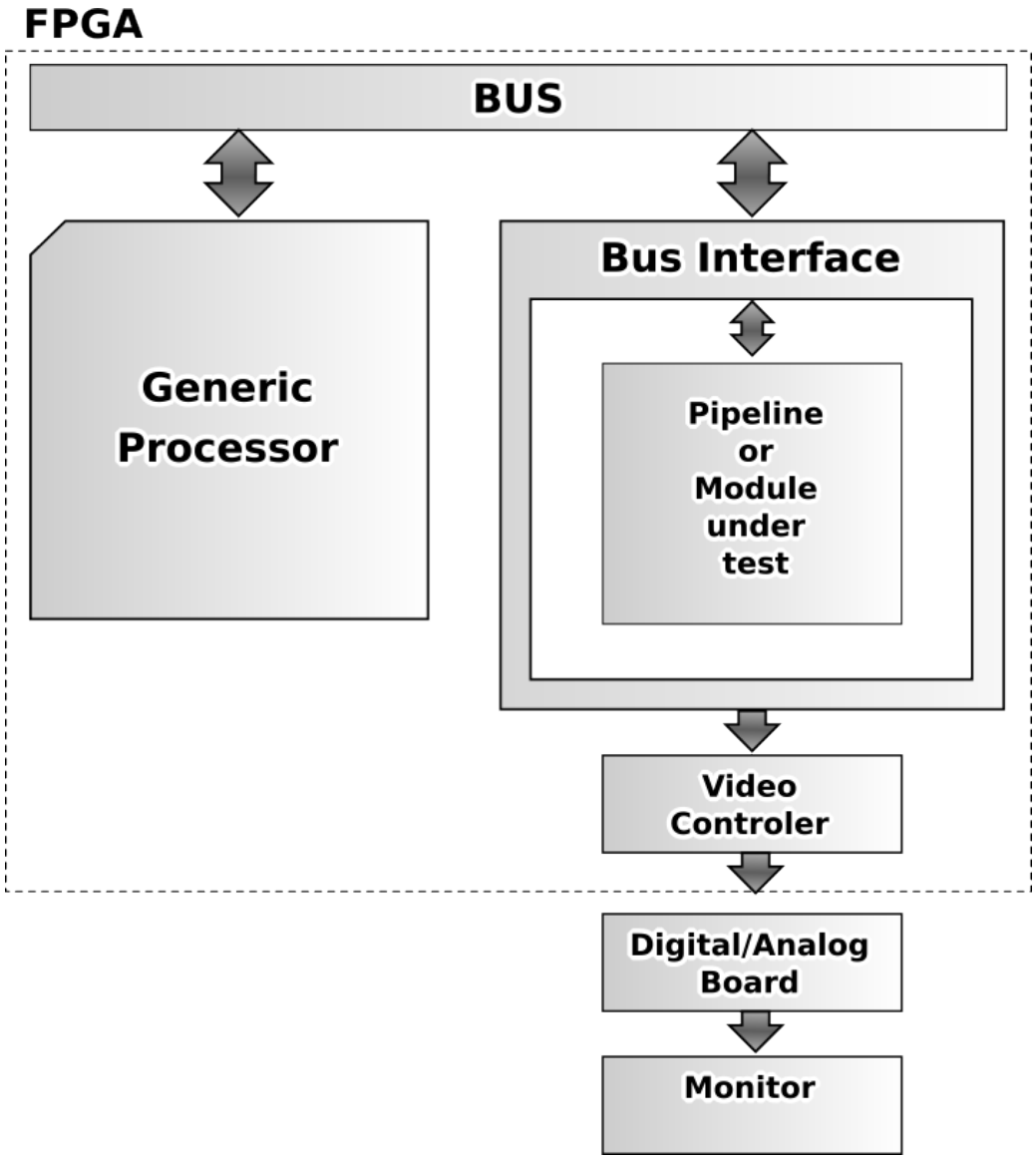


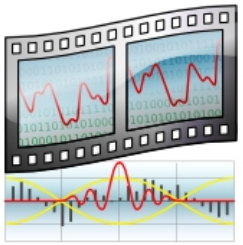
Data-path / pipeline

Each sub-module will be developed independently and can be tested with a direct bind to the software (even without the entire pipeline). For example, the IDCTSlow can be tested without the other sub-modules.

Later, all sub-modules will be integrated as the two described pipelines.

FPGA implementation





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